ADAU145X Product Data Sheet Revision

Item	Rev C	Rev D	Location
IOVDD Minimum Range	In the table headings it was incorrectly stated at IOVDD = 1.8V -10%. It is really -5%.	Changed the IOVDD minimum range in the text throughout the document. IOVDD = 1.8 V – 5%	Table 2, Table 3, and the top of most of the specification tables and many places in the Theory of Operation
DVDD Regulator MAX	N/A	Added the specification for the DVDD regulator output.	Table 3, Pg 8. Table 4 Pg 10
Digital Input/output Levels	ViH Min and ViL Max were improperly shown as the same voltage which is an error in the specification. This was only shown at the nominal voltages of 3.3V and 1.8V which is also not the best way to show this specification.	The change was to specify this over the valid range of IOVDD using an industry standard way of describing the digital levels. VoH and VoL where also changed to be specified over the full IOVDD range.	Table 5 Pg 11.
I2C Sink Current Specification	N/A	Added a specification for the maximum current that can be sunk on the I2C pins.	Table 5 Pg 11.
I2C R-on Spec	N/A	Added the ON-resistance specification for the I2C pins for the four different drive strengths.	Table 5 Pg 11.
Serial Port Output delay in slave mode verses Drive Strengths	N/A	Added the timing for the serial data output in slave mode, Tsods, at the four different drive strengths at 3.3V +/- 10%.	Table 9 Pg 14
Tsods	Tsods specification was shown to the rising edge of the bit clock instead of from the falling edge of the bitclock. The description in Table 8 was correct and the specification was correct but the figure did not properly show the measurement. (Figure 6, Page 10)	Correction to figure to show proper measurement	Figure 6 Pg 15
Figure 14	Typo in figure 14. The crystal frequency was listed as 12.2888 MHz	Correction to 12.288 MHz.	Figure 14 Pg 31
Initialization table	Table 24, Pg 26	Added some details to the initialization routing and clarified the text.	Table 27, Pg 32
Voltage Regulator Pass Transistor Selection	N/A	Added details about how to select a pass transistor and also about adding a series resistor if a ceramic bulk cap is used. These are applications details.	Page 40
SPI address format description	The bit numbers were backwards. Bit 7 is really bit 0 etc.	Correction to bit numbers	Table 36, Pg 47
SPDIF Receiver to Core	SPDIF Receiver to Core, Figure 45	Removed SPDIF Receiver to Core Figure 45 An ASRC must be used.	N/A
Programming the SigmaDSP Core Section	Programming the SigmaDSP Core Section	Updated Programming the SigmaDSP Core section Added details for applications. Added Table 60	Pages 90-91. Table 60

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Software Value Registers	Table 57 pg 79	Added the Software Value Panic registers that were previously hidden. These will be used soon for added features in SigmaStudio. Register addresses 0xF433 and 0xF434. These were also added to the register details section.	Table 61, Pg 92
Software Safeload Section	Changes to and Table 62	Made changes in the descriptions to reflect the recent changes in SigmaStudio to fix the safeload address. Backward compatibility was maintained so customer's software would not have to be changed unless they choose to.	Pg 93
Application section for Power Supply Regulator	Changes to Figure 86 page 177, Figure 88, pg 178	Updated Application section for Power Supply regulator drawings to be consistant with the theory of operation. Updated the Applications section and figure 86 to show the added series resistor to the DVDD bulk cap and also to fix some errors in figure 88 where 1uf caps were shown in error and there was one cap in the drawing which should not have been in the drawing.	Figure 86 Pg 192, Figure 88 Pg 193
ASRC Lock Bits	ASRC Lock Bits incorrect Table 120, Page 140	The ASRC_LOCK bit descriptions. This behavior of the ASRCs was changed from Rev B to Rec C silicon.	Table 126, Pg 154
Table 9 for MP Pins	Error in Table 9 page 11	Changed to divided by the Core frequency Rate. Slower core rate devices were added.	Table 10, Pg 15
Redundant data	Table 19, page 17	Deleted redundant rows of data. Consolidated redundancies into one row.	Table 20, Pg 21
Incorrect information in the table 26	Table 26 on page 29 incorrect.	Table 26 had the calculation of maximum instructions per sample incorrect. There was an extra zero on several of the system clock entries for 147.456 and 146.7648 MHz calculations.	Table 29, Pg 36
Memory Map Tables	Memory Map tables had incorrect data. Table 62 and 63, Pg 83	Corrected memory maps for the ADAU1451 and the ADAU1450. Corrected numbers for the length of DM0 and DM1.	Table 66 and 67, Pg 96
The Kill Core Register	Kill Core Register 0xF403 description. Pg 121	The Kill Core description was not clear that the core will remain killed as long as this bit is high. The decription was updated to add some functional detail	Pg 135